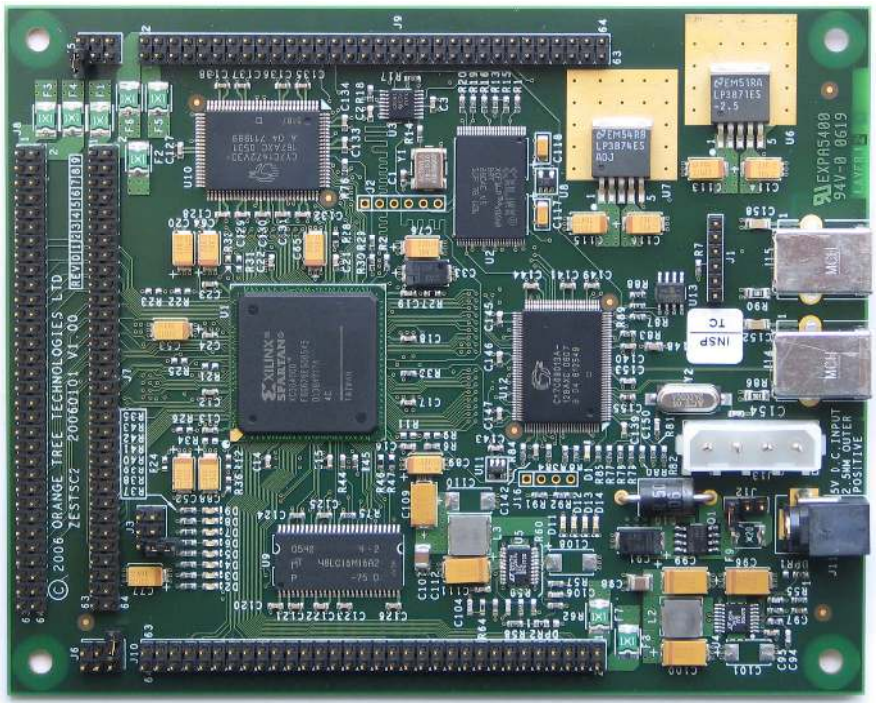
Orange Tree Technologies

ZestSC2: FPGA+USB Module

The ZestSC2 is a high performance, high specification FPGA module that connects to a host PC through High Speed USB 2.0 (480Mbits/s) and achieves a sustained USB bandwidth of 38MBytes/s. The board has a compact form factor (150 x122mm) and is intended for applications such as semiconductor prototyping and test , DAQ, industrial control and image processing. It can also be used as a desk-top board for advanced FPGA based prototyping, development, training and demonstrations.

Feature rich, the ZestSC2 is fitted with a high density Xilinx Spartan-3 FPGA with up to 4 million gates. There are also 64MBytes SDRAM, 8MBytes of pipelined ZBT SRAM, FPGA configuration flash memory and 200 header pins for user I/O. The board can be powered entirely from the USB port, there is a secondary power only USB port, or if more than 5W is required there is a wall adapter or hard disk drive power connector. The board features standard 0.1” pitch connectors for maximum flexibility.

Provided with the ZestSC2 are libraries and IP to support an out-of-the-box experience. This includes: host support software including a system driver and a host library; USB interface; SRAM and SDRAM interfaces; HDL testbenches; multiple design examples that consists of a host program and a VHDL and Verilog project (including source). All the board needs to operate is a USB cable connected to a PC.



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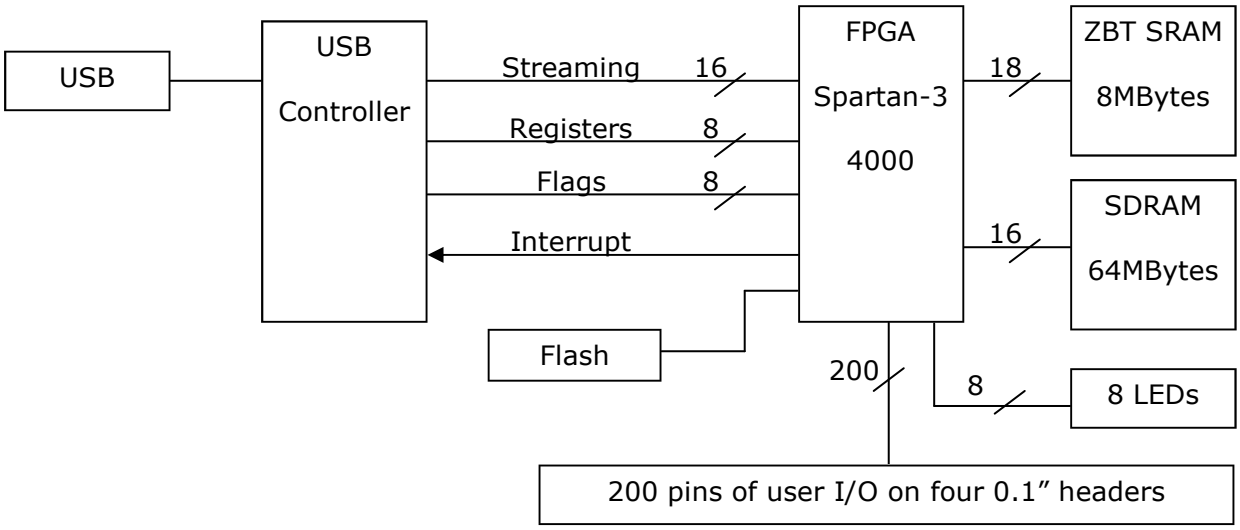

USB	High Speed USB 2.0 (480Mbits/s burst, up to 38MBytes/s sustained (dependent on host)) or Full Speed USB 1.1 (12Mbits/s burst). Cypress EZ-USB FX2 USB microcontroller chip.
FPGA	Xilinx Spartan-3 XC3S4000-5 in FGG676 package Configured from USB, Flash or Xilinx Parallel Cable IV with JTAG
Host communications	Three interfaces between FX2 and FPGA all accessible using host library supplied with board: Streaming—data streaming at the maximum USB bandwidth; Registers—control and status registers in FPGA application; Signalling—single bit interrupt and flags.
Memory	SDRAM 32M x 16 Pipelined ZBT SRAM 4M x 18—ZBT is "Zero Bus Turnaround" for no wait states between writes and reads FPGA configuration Flash memory
I/O	Four 64-pin 0.1" headers for ribbon cable or daughter card (for example ADC/DAC, video) Two headers with 49 pins and two with 51 pins connected to FPGA for user I/O Multiple grounds, 1 pin 5V, 1 pin jumper selectable FPGA I/O voltage (3.3V, 2.5V or user settable) on each connector.
LED's	8 LED's connected to FPGA I/O pins, active low 4 LED's for power indication, 1 LED for FPGA Done signal
FPGA Clocks	Fixed 48MHz for streaming interface between FX2 and FPGA Fixed 48MHz for microcontroller registers interface between FX2 and FPGA I/O input clock from I/O header—single ended or differential FPGA can synthesise internal clocks from 1.5MHz to 280MHz from the above clock inputs
Power	Up to 95% efficient on-board 10W PSU enables the board to be either bus-powered from a high power USB port; or self-powered from a wall adapter or hard disk power connector (both nominal 5V) for higher power applications or when a low power USB port is used. Secondary USB port enables up to 5W to be supplied from host PC
Software	Host library and drivers for configuring FPGA and communicating with the FPGA, which run on Windows and Linux, for other operating systems please enquire
Logic cores	FPGA interfaces for FX2, SDRAM and SRAM—cores and testbenches in both VHDL and Verilog
Examples	C, VHDL and Verilog source code for various examples
Physical	150 x 122 mm

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